Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

1-30. (Canceled)

31. (Currently amended): A memory access method in a data processing unit comprising dynamic memory and re-programmable non-volatile memory, the method comprising:

detecting a write operation to an area in the re-programmable non-volatile memory;

determining a caching location which identifies an area of memory in ~~a~~ the dynamic memory to which data to be written by the write operation can be cached, the area of memory identified by the caching location referred to as a caching area; and

writing the data to the caching area instead of writing the data to the area in the re-programmable non-volatile memory,

wherein the caching area is associated with the area in the re-programmable non-volatile memory.

32. (Currently amended): The method of claim 31 wherein the step of determining a caching location comprises:

determining if ~~the data can be stored in~~ the dynamic memory has capacity to store the data, and if not then:

identifying one or more memory locations in the dynamic memory; and

writing content in the one or more memory locations to the re-programmable non-volatile memory; and

providing an address in the dynamic memory as the caching location in the area of memory.

33. (Original): The method of claim 32 wherein the step of determining a caching location in the dynamic memory is limited to determining a caching location in a segment of the dynamic memory.

34. (Original): The method of claim 31 further including detecting a second write operation to the area in the re-programmable non-volatile memory and writing the data associated with the second write operation to the area of memory identified by the caching location instead of writing the data to the area in the re-programmable non-volatile memory.

35. (Original): The method of claim 31 further including detecting a second write operation to a second area in the re-programmable non-volatile memory, determining if there is a caching area in the dynamic memory that is associated with the second area and if there is then writing data associated with the second write operation to the caching area associated with the second area.

36. (Original): The method of claim 31 wherein an address space of the re-programmable non-volatile memory is equal to or greater than an address space of the dynamic memory.

37. (Original): The method of claim 32 wherein the step of identifying one or more memory locations is based on the size of the data.

38. (Original): The method of claim 32 wherein the step of identifying one or more memory locations is based on contents of the data.

39. (Original): The method of claim 38 wherein the step of identifying one or more memory locations includes applying a hash function on the data to produce a hash result, the one or more locations determined based on the hash result.

40. (Currently amended): The method of claim 31 wherein the re-programmable non-volatile memory is one of an EEPROM (electrically erasable programmable read-only memory) ~~and~~ or a flash memory.

41. (Original): The method of claim 31 further including obtaining an address range which defines the area of memory in the dynamic memory.

42. (Original): The method of claim 31 further including detecting a read operation from the re-programmable non-volatile memory and reading the re-programmable non-volatile memory to effect the read operation.

43. (Original): The method of claim 31 further including detecting a read operation from the re-programmable non-volatile memory and reading one or more memory locations from the area of memory in the dynamic memory to effect the read operation.

44. (Currently amended): A data processing unit comprising:

a dynamic memory;

a memory bus for accessing ~~a~~ the dynamic memory;

a re-programmable non-volatile memory;

memory access logic operatively coupled to the memory bus and to the re-programmable non-volatile memory; and

processor logic operatively coupled to the memory access logic to transfer data with the dynamic memory via the memory bus and to transfer data with the re-programmable non-volatile memory,

the memory access logic configured to detect a write operation to the re-programmable non-volatile memory,

the processor logic configured to respond to the memory access logic detecting the write operation and to:

identify a caching location in ~~the area of~~an area of the dynamic memory wherein data to be written by the write operation can be cached; and

store the data in the area of the dynamic memory identified by the caching location.

45. (Currently amended): The data processing unit of claim 44 wherein the ~~memory access~~processor logic is further configured to:

determine if ~~the data can be stored in~~ the area of the dynamic memory has capacity to store the data; and

provide an address in the area of the dynamic memory as the caching location ~~in the area of memory~~,

wherein if it is determined that the caching location lacks capacity to store the data~~data cannot be stored in the area of memory~~, then:

identify one or more other memory locations in the area of the dynamic memory; and

write content in the one or more other memory locations to the re-programmable non-volatile memory,

wherein the one or more other memory locations ~~are~~ become available for caching a write operation.

46. (Original): The data processing unit of claim 44 wherein an address space of the re-programmable non-volatile memory is equal to or greater than an address space of the dynamic memory.

47. (Currently amended): The data processing unit of claim 44 wherein the re-programmable non-volatile memory is one of an EEPROM (electrically erasable programmable read-only memory) ~~and~~ or a flash memory.

48. (Original): The data processing unit of claim 44 wherein the dynamic memory is a random access memory.

49. (Original): The data processing unit of claim 44 wherein the memory access logic is further configured to detect a read operation from the re-programmable non-volatile memory and to effect a read operation therefrom.

50. (Original): The data processing unit of claim 44 wherein the memory access logic is further configured to detect a read operation from the re-programmable non-volatile memory and to access the area in memory in the dynamic memory to effect the read operation.

51. (Original): A memory access method comprising:

detecting a write operation to a re-programmable non-volatile memory; and

if a destination address associated with the write operation is within a first range of addresses, then performing a fast write operation of data associated with the write operation to the re-programmable non-volatile memory.

52. (Original): The method of claim 51 wherein the first range of addresses spans the entire address space of the re-programmable non-volatile memory.

53. (Original): The method of claim 51 wherein if the destination address is not within the first range of addresses, then performing a slow write operation of the data to the re-programmable non-volatile memory.

54. (Original): The method of claim 51 wherein the first range of addresses spans a range of addresses less than the address space of the re-programmable non-volatile memory.

55. (Original): The method of claim 51 wherein the step of performing a fast write operation is performed if the destination address falls within any of a plurality of ranges of addresses.

56. (Original): A memory access method comprising:

detecting a write operation to a non-volatile memory;

determining an access mode;

if the access mode is a first mode, then performing a fast write operation of data associated with the write operation to the non-volatile memory;

if the access mode is a second mode, then performing a slow write operation of the data associated with the write operation; and

if the access mode is a third mode, then:

if the destination address associated with the write operation is within a first range of addresses, then performing a fast write operation of the data associated with the write operation to the non-volatile memory;

if the destination address is not within the first range of addresses, then performing a slow write operation of the data to the non-volatile memory; and

if the access mode is a fourth mode, then:

determining a caching location which identifies an area of memory in a dynamic memory to which data to be written by the write operation can be cached, the area of memory identified by the caching location referred to as a caching area; and

writing the data to the caching area instead of writing the data to the area in the non-volatile memory,

wherein the caching area is associated with the area in the non-volatile memory.

57-62. (Canceled)

63. (Original): A memory access method for accessing a re-programmable non-volatile memory comprising:

detecting a write operation to the re-programmable non-volatile memory, the write operation having an associated destination address and associated one or more data to be written to the re-programmable non-volatile memory;

determining an operating mode;

if the operating mode indicates a first mode of operation, then:

performing a partial write operation of each datum to the re-programmable non-volatile memory, if the destination address is within a first range of addresses; and

performing a full write operation of each datum to the re-programmable non-volatile memory, otherwise;

if the operating mode indicates a second mode of operation, then performing a full write operation of each datum to the re-programmable non-volatile memory;

if the operating mode indicates a third mode of operation, then performing a partial write operation of each datum to the re-programmable non-volatile memory; and

if the operating mode indicates a fourth mode of operation, then:

determining a caching location which identifies an area of memory in a dynamic memory where the data can be cached; and

writing the data in the area of memory identified by the caching location instead of writing to the re-programmable non-volatile memory.

64. (Currently amended): The method of claim 63 wherein the re-programmable non-volatile memory is one of an EEPROM (electrically erasable programmable read-only memory) ~~and~~ or a flash memory.